(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 502 532 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
24.05.2000 Bulletin 2000/21

(51) Int. Cl.[7]: **G06F 12/14**

(21) Application number: **92103791.7**

(22) Date of filing: **05.03.1992**

(54) Single chip microcomputer having protection function for content of internal ROM

Einchipmikrorechner mit Schutzfuntion für den Inhalt eines internen ROM's

Microordinateur monopuce avec fonction de protection pour le contenu d'une mémoire morte interne

(84) Designated Contracting States:
DE FR GB

(30) Priority: **06.03.1991 JP 3964191**

(43) Date of publication of application:
09.09.1992 Bulletin 1992/37

(73) Proprietor: **NEC CORPORATION**
Tokyo (JP)

(72) Inventor:
Iwamoto, Shinichi,
c/o NEC Corporation
Minato-ku, Tokyo (JP)

(74) Representative:
Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(56) References cited:
EP-A- 0 136 155
EP-A- 0 308 219
US-A- 4 153 933

EP 0 502 532 B1

Description

Background of the Invention

Field of the invention

[0001] The present invention relates to a single chip microcomputer, and more specifically to a single chip microcomputer having a function of protecting secrecy of a content of an internal ROM.

Description of related art

[0002] Some conventional single chip microcomputers have an internal ROM (read only memory) operation mode and an external memory operation mode. In this type of single chip microcomputer, an address discriminating circuit is provided internally in the single chip microcomputer so as to discriminate whether an address on an internal address bus is directed to an internal ROM or an external memory via a respective selector. If the address is directed to the internal ROM, the address discriminating circuit controls an associated selector to cause it to select the internal ROM, so that for example a CPU (central processing unit) can access to the internal ROM. If the address is directed to the external memory, the address discriminating circuit controls the selector to cause it to select the external memory, so that the CPU can access to the external memory via said selector.

[0003] In addition, there is provided an operation mode designating terminal which is accessible from an external. If the operation mode designating terminal is brought to an external memory operation mode designation level, the address discriminating circuit controls the selector to select the external memory, regardless of the address on the internal address bus.

[0004] Generally, the external memory has an address space considerably larger than that of the internal ROM. In some cases, a program for reading out a content of the internal ROM is stored in the external memory at a location having an address different from that of the internal ROM. In this case, if the CPU is initialized and the operation mode designating terminal is set to the external memory operation mode designation level, a programmed operation is started from a heading address of the external memory. If the program for reading out the content of the internal ROM starts from the heading address of the external memory, the internal ROM reading program is executed. In the course of execution of this reading program, even if the level of the operation mode designating terminal is changed from the external memory operation mode designation level to an internal ROM operation mode designation level, since the address storing the internal ROM reading program is out of an address area of the internal ROM, the address discriminating circuit continues to control the selector to cause it to select the program data stored in the external memory, so that the reading program stored in the external memory is continuously executed.

[0005] Further, when the operation mode designating terminal is set to the internal ROM operation mode designation level, if an instruction for sequentially reading the data stored in the internal ROM is executed in the course of execution of the program, since an address to he read is in the address area of the internal ROM, the address discriminating circuit controls the selector to cause it to select the output of the internal ROM. Therefore, the data of the internal ROM is sent through an internal data bus to an external data bus.

[0006] Namely, the data stored in the internal ROM of the single chip microcomputer can be easily read out by even a third party by means of the program stored in the external memory, by handling the level of the operation mode designating terminal. This is disadvantageous since even a third party can read out the data and therefore the software lacks secrecy.

[0007] From EP-A-01 36 155 is known a single chip microcomputer including an internal ROM as well as an external memory connected to the microcomputer through an interface terminal. The selection of one of the memories is done in accordance with a logical value which is latched when the resetting mode is released.

[0008] Accordingly, it is the object of the present invention to provide a microcomputer which overcomes the above-mentioned defects and which is capable of maintaining the secrecy of a content of data in an internal ROM.

[0009] This object is achieved by means of the features of the main claim.

[0010] Further advantageous features are mentioned in the sub-claims.

[0011] The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

[0012]

Figure 1 is a block diagram of a single chip microcomputer in accordance with the present invention;
Figure 2 shows a location of the program for reading the internal ROM
Figure 3 is a block diagram of an embodiment of the single chip microcomputer in accordance with the present invention; and
Figure 4 shows a location of the program for reading the internal ROM of the embodiment.

Description of the Preferred embodiments

[0013] Referring to Figure 1, there is shown a block diagram of a single chip microcomputer. As shown in

Figure 1, a single chip microcomputer 1 is coupled to an external memory 7, and comprises an address discriminating circuit 2, an internal ROM 3, a selector 4, a CPU 5 and a latch circuit 6, which are coupled as shown. The latch circuit 6 can be formed of for example a D-type flip-flop. The other components including an internal RAM and a timer circuit are not shown in Figure 1 because they does not directly relate to the present invention.

[0014] Through an internal address bus 201, an address information is transferred to the address discriminating circuit 2 and the internal ROM 3 of the single chip microcomputer 1, and also to the external memory 7 through an address bus interface terminal 40 and an external address bus 204. An output of the internal ROM 3 is connected to one input of the selector 4, and the other input of the selector 4 is connected to an internal data bus 202, which is connected to the CPU 5 and also through a data bus interface terminal 41 and an external data bus 203 to the external memory 7. Therefore, the CPU 5 receives the program data and the processing data on the internal data bus 202, and executes a processing on the basis of the received program/processing data. The CPU 5 is also connected to a reset terminal 52 so that the CPU 5 is initialized when the reset terminal 52 is brought to a resetting level. The reset signal supplied from the reset terminal 52 is also supplied to other functional blocks (not shown) within the single chip microcomputer 1.

[0015] The address discriminating circuit 2 also receives an output Q of the latch circuit 6. The latch circuit 6 receives at its data terminal D an operation mode designation signal supplied from an operation mode designating terminal 51 and also receives at its toggle input T the reset signal supplied from the reset terminal 52. The latch circuit 6 functions to maintain the level of tile operation mode designating terminal 51 when the resetting is released. Namely, the latch circuit 6 latches the level of the operation mode designating terminal 51 at the moment the level of the reset signal constituting the toggle input of the latch circuit 6 is caused to change from a resetting level to a non-resetting level.

[0016] When the output of the latch circuit 6 is at an external memory operation mode designation level (called an "Ex level" hereinafter), the address discriminating circuit 2 generates to the selector 4 a level signal having a first level causing it to select the external memory 7, regardless of the address information on the internal address bus 201. When the output of the latch circuit 6 is at an internal ROM operation mode designation level (called an "Int level" hereinafter), the address discriminating circuit 2 discriminates whether the received address information designates the internal ROM 3 or the external memory 7. When the received address is directed to the internal ROM 3, the address discriminating circuit 2 outputs the level signal having a second level to the associated selector 4 to cause it to select the internal ROM 3. When the received address is directed to the external memory 7, the address discriminating circuit 2 outputs the level signal having the first level to the selector 4 to cause it to select the external memory 7.

[0017] The external memory 7 sends to the external data bus 203 the processing data read out in accordance with an address information supplied to the external memory 7 through the address bus interface terminal 40 of the single chip microcomputer I and the external address bus 204. Through the external data bus 203, the processing data outputted from the external memory, 7 is transferred to the date bus interface terminal 41 of the single chip microcomputer 1 and therefore to the internal data bus 202. On the other hand, data outputted onto the internal data bus 202 can be transferred through the date bus interface terminal 41 and the external data bus 203 to the external memory 7.

[0018] Then, an operation for reading data stored in the internal ROM 3 in the above mentioned single chip microcomputer will be described.

[0019] First, as illustrated in the location of the reading program shown in Figure 2, assume that an addressable space in the single chip microcomputer is 64 kilobytes having the addresses form 0 to $FFFF_H$ (where the suffix "h" means the hexadecimal notation) and that the capacity of the internal ROM 3 is 16 kilobytes, and also assume that a program for reading the internal ROM 3 is stored in the external memory 7 at addresses which are not mapped to the internal ROM 3 (the addresses starting at the address 5000_H in Figure 2). In addition, a heading address (5000_H in Figure 2) of the reading program is also set in a reset vector table for setting a program start address after a resetting.

[0020] The program for reading the data of the internal ROM 3 is very simple: After the output level of the latch circuit 6 is changed to the internal ROM operation mode designation level, an instruction for reading the internal ROM 3 is executed. The read-out data is stored in an external RAM (not shown) through the external data bus 203 or read through a predetermined output port.

[0021] The internal ROM reading program as mentioned above is stored in the external memory 7, and the operation is started when the reset signal for initialization is inputted from the reset terminal 52 while the operation mode designating terminal 51 is at the Ex level for designating the external memory operation mode (and therefore, the Q output of the latch circuit 6 is also at the Ex level). Here, if the Ex level is at a low level, this Ex level can be easily set, for example, by connecting a pull-down resistance to the operation mode designating terminal 51.

[0022] The execution of the reading program is started from the heading address of the reading program in accordance with the reset vector table set in the external memory 7. In the course of execution of this program, namely, after the release of the resetting, even if the level at the operation mode designating terminal

51 is changed, the output of the Q terminal of the latch circuit 6 does not change, and therefore, the action of the address discriminating circuit 2 does not change. Thus, when the operation is started in the external memory operation mode in the case of the reading program, the operation mode cannot be changed to the internal ROM operation mode in the course of execution of the program, and therefore, it is impossible to read the data stored in the internal ROM 3. Accordingly, the addition of the latch circuit 6 enables it to very easily maintain the secrecy of the content of data in the internal ROM 3.

[0023] Now, an embodiment of the microcomputer in accordance with the present invention will be described with reference to Figure 3, which shows a block diagram of the second embodiment. In Figure 3, elements similar to those shown in Figure 1 are given the same Reference Numerals, and explanation thereof will be omitted. Further, Figure 4 shows a location of the reading program of the internal ROM in the second embodiment.

[0024] As shown in Figure 3, the single chip microcomputer 1 of the embodiment coupled to the external memory 7 comprises the address discriminating circuit 2, the internal ROM 3, the selector 4, the CPU 5, the latch circuit 6, output port latches 8 and 9, selectors 10 and 11, a memory extension flag 12 and an AND circuit 13, which are coupled as shown.

[0025] The circuit of the embodiment is more practical than that above mentioned microprocessor. The circuit of this embodiment is different from that of fig.1 in that it additionally includes the selectors 10 and 11 and the output ports 8 and 9 so that the interface terminal can be used as a port in the case of not using the external memory 7 and in that the second embodiment comprises the memory extension flag 12, which makes it possible to operate with respect to an external device in a more elaborate way.

[0026] With reference to Figures 3 and 4, operation of the address discriminating circuit 2 and the selectors 4, 10 and 11 in combination with the operation mode designating terminal 51 and the memory extension flag 12 will be described. In Figure 4, the addressable range is mapped to 64 kilobytes of 0 to $FFFF_H$, and the internal ROM 3 is mapped to 16 kilobytes of 0 to $3FFF_H$.

[0027] When the resetting is released, if the operation mode designation terminal 51 is at the Ex level of "0", the Ex level of "0" is latched in the latch circuit 6, and therefore, the address discriminating circuit 2 controls the selector 4 to select the data from the external data bus 203, regardless of the address information, and the selector 4 sends the selected data to the internal data bus 202. At this time, since the output of the AND circuit 13 is at "0" similarly to the Ex level, regardless of the level of the memory extension flag 12, the internal address bus 201 and the internal data bus 202 are connected to corresponding interface terminals 40 and 41 by the selectors 10 and 11, respectively, in accordance with the output "0" of the AND circuit 13. Thus, as shown in Figure 4, it operates only by the external memory 7, regardless of the address value.

[0028] When the level of the operation mode designating terminal 51 latched in the latch circuit 6 is "1" and the output level of the memory extension flag 12 is "0", the selector 4 is controlled in accordance with the level signal outputted from the address discriminating circuit 2, so as to select the data from the internal ROM 3 if the address information is in the range of 0 to $3FFF_H$ and the data from the external memory 7 if it is in the range of 4000_H to $FFFF_H$. In this case, since the output of the AND circuit 13 is "0" similarly to the Ex level, the selectors 10 and 11 select the internal address bus 201 and the internal data bus 202, respectively. Thus, as shown in Figure 4, it is possible to access both of the internal ROM 3 and the external memory 7 in accordance with the address information.

[0029] Then, when the operation mode designating terminal 51 latched in the latch circuit 6 is at "1" while the output level of the memory extension flag 12 is at "1", the address discriminating circuit 2 controls the selector 4 so as to select the data from the internal ROM 3 if the address information is in the range of 0 to $3FFF_H$ and the data from the external memory 7 if it is in the range of 4000_H to $FFFF_H$. In this case, however, since the output of the AND circuit 13 is at "1" which is the same level as the Int level, the selectors 10 and 11 select the output port latches 8 and 9, respectively. Thus, as shown in Figure 4, the interface terminals 40 and 41 output the data latched in the output port latches 8 and 9, not the interface signal to the external memory 7. In this operation mode, therefore, the connection to the external memory 7 is not effected, and it is possible to use the interface terminals 40 and 41 as a port output terminal by means of the action in the range of the internal ROM 3.

[0030] Similarly to the embodiment of fig.1, the level of the operation mode designating terminal 51 at the moment the resetting is released is maintained in the latch circuit 6 as it is, and therefore, it is impossible to access the internal ROM 3 in the case that the operation was started with the external memory operation mode. Thus, the secrecy of the data stored in the internal ROM is maintained. On the other hand, if the operation was started with the internal ROM operation mode, it is possible to choose whether or not the external memory 7 is used, by rewriting a memory extension flag 12 by means of a programmed operation. Therefore, it is possible to modify the way of using it in accordance with application systems.

[0031] As mentioned above, the present invention has an effect that the secrecy of the content of data in the internal ROM can be kept by providing a latch circuit for latching the level at the operation mode designating terminal at the time of releasing the resetting.

[0032] The invention has thus been shown and described with reference to the specific embodiments.

However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. A single chip microcomputer (1) configured to be coupled to an external memory (7) through at least an external address bus (204) and an external data bus (203), the single chip microcomputer comprising:

an internal address bus (201) connected via a first selector (10) to an address interface terminal (40) which can be coupled to said external address bus (204);
an internal data bus (202) connected via a second selector (11) to a data interface terminal (41) which can be coupled to said external data bus (203);
an internal memory (3) coupled to said internal address bus (201);
a central processing unit (5) coupled to said internal data bus (202) and connected to a reset terminal (52); and
a latch circuit (6) having a data input connected to an operation mode designation terminal (51) and a latch timing control input connected to said reset terminal (52) so that that said latch circuit (6) latches a logical level on said operation mode designation terminal (51) when said reset terminal is brought from a resetting level to a non-resetting level,
a third selector (4) having a first input connected to an output of said internal memory (3) and a second input connected to said internal data bus (202), an output of said selector being connected to said internal data bus (202);
an address discriminating circuit (2) being coupled to said internal address bus (201) for discriminating whether an address on said internal address bus is directed to said internal memory (3) or said external memory (7) and for generating a selection signal to said third selector (4), so that when the address on said internal address bus (201) is directed to said internal memory (3), said address discriminating circuit (2) causes said selector (4) to select and output said output of said internal memory (3), and when the address on said internal address bus is directed to said external memory, said address disciminating circuit causes said selector (4) to select and output the data supplied to said internal data bus from said external memory (7);
an output of said latch circuit (6) being connected to said address discriminating circuit (2) so that when said output of said latch circuit indicates said external memory, said address disriminating circuit (2) causes said selector (4) to select and output the data supplied to said internal data bus from said external memory (7), regardless of the address on said internal address bus (201);
whereby, when the operation was started with an external memory operation mode, even if the logical value of said operation mode designation terminal is changed after the resetting is released, the output of said latch circuit does not change, and therefore, the operation mode is in no way changed to an internal ROM operation mode in the course of execution of a program, and
said first selector (10) having a first input connected to said internal address bus (201) and a second input connected to a first output port latch (8), an output of said second selector being connected to said address interface terminal (40),
said second selector (11) having a first input connected to said internal data bus (202) and a second input connected to a second output port latch (9), an output of said second selector (11) being connected to said data interface terminal (41), and
a logic gate (13) having a first input connected to a memory extension flag (12) and a second input connected to said output of said latch circuit (6), an output of said logic gate (13) being connected to a control input of each of said first and second selectors (10, 11), so that when said output of said latch circuit indicates said internal memory (3) and said memory extension flag (12) does not indicate a memory extension, said first and second output port latches (8, 9) are coupled to said address interface terminal (40) and said data interface terminal (41) through said first and second selectors (10, 11), respectively.

2. A single chip microcomputer claimed in claim 1, wherein said logic gate (13) is formed of an AND gate.

3. A single chip microcomputer claimed in claim 1, wherein said latch circuit (6) includes a D-type flipflop having a data input (D) connected to the operation mode designation terminal (51) and a toggle input (T) connected to said reset terminal (52), a Q output of said flipflop being connected to said address discriminating circuit (2).

Patentansprüche

1. Einchip-Mikrocomputer (1), geeignet zur Kopplung

an einen externen Speicher (7) über mindestens einen externen Adressbus (204) und einen externen Datenbus (203), welcher aufweist:

einen internen Adressbus (201), der über einen ersten Selektor (10) mit einem Adresseninterfaceanschluß (40) verbunden ist, welcher an den externen Adressbus (204) gekoppelt werden kann;
einen internen Datenbus (202), der über einen zweiten Selektor (11) mit einem Dateninterfaceanschluß (41) verbunden ist, welcher an den externen Datenbus (203) gekoppelt werden kann; einen internen Speicher (3), der an den internen Adressbus (201) gekoppelt ist;
eine zentrale Recheneinheit (5), die an den internen Datenbus (202) gekoppelt und mit einem Rücksetzanschluß (52) verbunden ist; und
eine Halteschaltung (6), deren Dateneingang verbunden ist mit einem Betriebsmodenbestimmungsanschluß (51), und dessen Haltesynchronisationssteuereingang verbunden ist mit dem Rücksetzanschluß (52), so daß die Halteschaltung (6) einen logischen Pegel an dem Betriebsmodusbestimmungsanschluß (51) hält, wenn der Rücksetzanschluß von einem Rücksetzpegel auf einen Nicht-Rücksetzpegel gebracht wird,
einen dritten Selektor (4) mit einem ersten Eingang, der mit einem Ausgang des internen Speichers (3) verbunden ist, und einem zweiten Eingang, der mit dem internen Datenbus (202) verbunden ist, wobei ein Ausgang des Selektors verbunden ist mit dem internen Datenbus (202);
einen Adressdiskriminatorschaltkreis (2), der mit dem internen Adressbus (201) verbunden ist, um zu entscheiden, ob eine Adresse auf dem internen Adressbus an den internen Speicher (3) oder den externen Speicher (7) gerichtet ist und zum Erzeugen eines Wahlsignals für den dritten Selektor (4), so daß, wenn die Adresse auf dem internen Adressbus (201) an den internen Speicher (3) gerichtet ist, der Adressdiskriminatorschaltkreis (2) verursacht, daß der Selektor (4) den Ausgang des internen Speichers (3) auswählt und ausgibt, und wenn die Adresse des internen Adressbuses an den externen Speicher gerichtet ist, der Adressdiskriminatorschaltkreis verusacht, daß der Selektor die von dem externen Speicher (7) an den internen Bus zugeführten Daten auswählt und ausgibt;
wobei ein Ausgang des Halteschaltkreises (6) verbunden ist mit dem Adressdiskriminatorschaltkreis (2), so daß, wenn der Ausgang des Halteschaltkreises den externen Speicher anzeigt, der Adressdiskriminatorschaltkreis (2) verursacht, daß der Selektor (4) die vom externen Speicher (7) an dem internen Datenbus zugeführten Daten auswählt und ausgibt, unabhängig von der Adresse auf den internen Adressenbus (201);
wodurch, wenn der Betrieb gestartet wurde mit einem externen Speicherbetriebsmodus, selbst wenn der logische Wert des Betriebsmodusbestimmungsanschlusses geändert wird, nachdem das Rücksetzen aufgehoben wurde, der Ausgang des Halteschaltkreises sich nicht ändert, und deshalb der Betriebsmodus geändert wird auf keine Weise auf einen internen ROM-Betriebsmodus während der Ausführung eines Programmes, und
wobei der erste Selektor (10) einen ersten Eingang hat, der mit dem internen Adressbus (201) verbunden ist, und einen zweiten Eingang, der mit einem ersten Ausgangsporthaltekreis (8) verbunden ist, wobei ein Ausgang des zweiten Selektors verbunden ist mit dem Adressinterfaceanschluß (40),
wobei der zweite Selektor (11) einen ersten Eingang hat, der mit dem internen Datenbus (202) verbunden ist und einen zweiten Eingang, der mit einer Zweiten Ausgangsport-Halteschaltung (9) verbunden ist, wobei der Ausgang des zweiten Selektors (11) mit dem Dateninterfaceanschluß (41) verbunden ist, und
ein logisches Gate (13), das einen ersten Eingang hat, der mit einer Speichererweiterungsflag (12) verbunden ist, und einen zweiten Eingang, der mit dem Ausgang des Halteschaltkreises (6) verbunden ist, wobei ein Ausgang des logischen Gates (13) verbunden ist mit einem Steuereingang jedes des ersten und zweiten Selektors (10, 11), so daß, wenn der Ausgang des Halteschaltkreises den internen Speicher (3) anzeigt und das Speichererweiterungsflag (12) keine Speichererweiterung anzeigt, die ersten und zweiten Ausgangsporthaltekreise (8, 9) über die ersten und zweiten Selektoren (10, 11) mit dem Adressinterfaceanschluß (40) bzw. dem Dateninterfaceanschluß (41) verbunden werden.

2. Ein-Chip-Mikrocomputer nach Anspruch 1, wobei das logische Gate (13) aus einem AND-Gate gebildet ist.

3. Einchip-Mikrocomputer nach Anspruch 1, wobei der Halteschaltkreis (6) einen D-Flip-Flop aufweist mit einem Dateneingang (D), der mit dem Betriebsmodus-Bestimmungsanschluß (51) verbunden ist, und einem Toggeleingang (T), der mit dem Rücksetzanschluß (52) verbunden ist, wobei

der Q-Ausgang des Flip-Flops mit dem Adressendiskriminatorschaltkreis (2) verbunden ist.

Revendications

1. Micro-ordinateur monopuce (1) configuré pour être couplé à une mémoire externe (7) par au moins un bus d'adresses externe (204) et un bus de données externe (203), le micro-ordinateur monopuce comprenant :

   - une bus d'adresses interne (201) connecté via un premier sélecteur (10) à une borne d'interface d'adresse (40) qui peut être couplée audit bus d'adresses externe (204) ;
   - un bus de données interne (202) connecté via un deuxième sélecteur (11) à une borne d'interface de données (41) qui peut être couplée audit bus de données externe (203) ;
   - une mémoire interne (3) couplée audit bus d'adresses interne (201) ;
   - une unité centrale de traitement (5) couplée audit bus de données interne (202) et connectée à une borne de remise à zéro (52) ;
   - un circuit de verrouillage (6) ayant une entrée de données connectée à une borne de désignation de mode de fonctionnement (51) et une entrée de commande d'horloge de verrouillage connectée à ladite borne de remise à zéro (52) de telle sorte que ledit circuit de verrouillage (6) verrouille un niveau logique sur ladite borne de désignation de mode de fonctionnement (51) lorsque ladite borne de remise à zéro passe d'un niveau de remise à zéro à un niveau de non-remise à zéro ;
   - un troisième sélecteur (4) ayant une première entrée connectée à une sortie de ladite mémoire interne (3) et une seconde entrée connectée audit bus de données interne (202), une sortie dudit sélecteur étant connectée audit bus de données interne (202) ; et
   - un circuit de discrimination d'adresse (2) qui est couplé audit bus d'adresses interne (201) pour discriminer si une adresse sur ledit bus d'adresses interne s'adresse à ladite mémoire interne (3) ou à ladite mémoire externe (7) et pour générer une signal de sélection vers ledit troisième sélecteur (4), de telle sorte que lorsque l'adresse sur ledit bus d'adresses interne (201) s'adresse à ladite mémoire interne (3), ledit circuit de discrimination d'adresse (2) fait en sorte que ledit sélecteur (4) sélectionne et sort ladite sortie de ladite mémoire interne (3), et lorsque l'adresse sur ledit bus d'adresses interne s'adresse à ladite mémoire externe, ledit circuit de discrimination d'adresse fait en sorte que ledit sélecteur (4) sélectionne et sort les données fournies audit bus de données interne depuis ladite mémoire externe (7) ;

     une sortie dudit circuit de verrouillage (6) étant connectée audit circuit de discrimination d'adresse (2) de telle sorte que lorsque ladite sortie dudit circuit de verrouillage indique ladite mémoire externe, ledit circuit de discrimination d'adresse (2) fait en sorte que ledit sélecteur (4) sélectionne et sort les données fournies audit bus de données interne depuis ladite mémoire externe (7), indépendamment de l'adresse sur ledit bus d'adresses interne (201) ;
     de telle manière que, lorsque le fonctionnement a commencé avec un mode de fonctionnement de mémoire externe, même si la valeur logique de ladite borne de désignation de mode de fonctionnement change après que la remise à zéro a été libérée, la sortie dudit circuit de verrouillage ne change pas, et par conséquent, le mode de fonctionnement n'est en aucune façon changé en un mode de fonctionnement de ROM interne au cours de l'exécution d'un programme, et

   - ledit premier sélecteur (10) ayant une première entrée connectée audit bus d'adresses interne (201) et une seconde entrée connectée à un premier circuit de verrouillage de port de sortie (8), une sortie dudit deuxième sélecteur étant connectée à ladite borne d'interface d'adresse (40),
   - ledit deuxième sélecteur (11) ayant une première entrée connectée audit bus de données interne (202) et une seconde entrée connectée à un second circuit de verrouillage de port de sortie (9), une sortie dudit deuxième sélecteur (11) étant connectée à ladite borne d'interface de données (41), et
   - une porte logique (13) ayant une première entrée connectée à un drapeau d'extension de mémoire (12) et une seconde entrée connectée à ladite sortie dudit circuit de verrouillage (6), une sortie de ladite porte logique (13) étant connectée à une entrée de commande de chacun desdits premier et deuxième sélecteurs (10, 11), de telle sorte que lorsque ladite sortie dudit circuit de verrouillage indique ladite mémoire interne (3) et ledit drapeau d'extension de mémoire (12) n'indique pas une extension de mémoire, lesdits premier et second circuits de verrouillage de port de sortie (8, 9) sont couplés à ladite borne d'interface d'adresse (40) et à ladite borne d'interface de données (41) par l'intermédiaire desdits premier et deuxième sélecteurs (10, 11), respecti-

vement.

2. Micro-ordinateur monopuce selon la revendication 1, dans lequel ladite porte logique (13) est formée d'une porte ET.

3. Micro-ordinateur monopuce selon la revendication 1, dans lequel ledit circuit de verrouillage (6) comporte une bascule bistable du type D ayant une entrée de données (D) connectée à la borne de désignation de mode de fonctionnement (51) et une entrée de basculement (T) connectée à ladite borne de remise à zéro (52), une sortie Q de ladite bascule bistable étant connectée audit circuit de discrimination d'adresse (2).

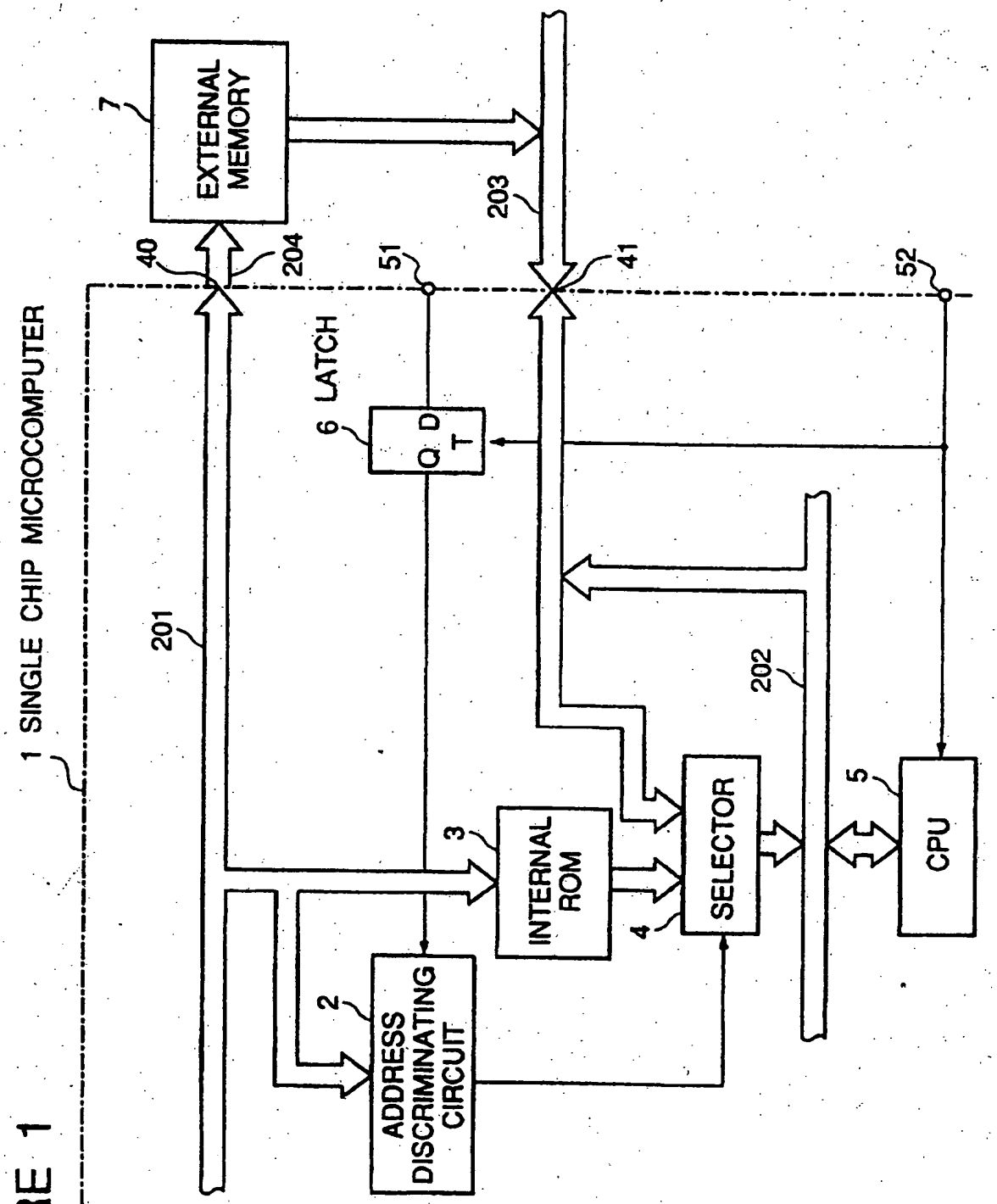

1 SINGLE CHIP MICROCOMPUTER
EXTERNAL MEMORY
7
40
204
203
51
41
52
6 LATCH
D
Q
T
201
202
INTERNAL ROM
3
SELECTOR
4
CPU
5
ADDRESS DISCRIMINATING CIRCUIT
2

FIGURE 1

FIGURE 2

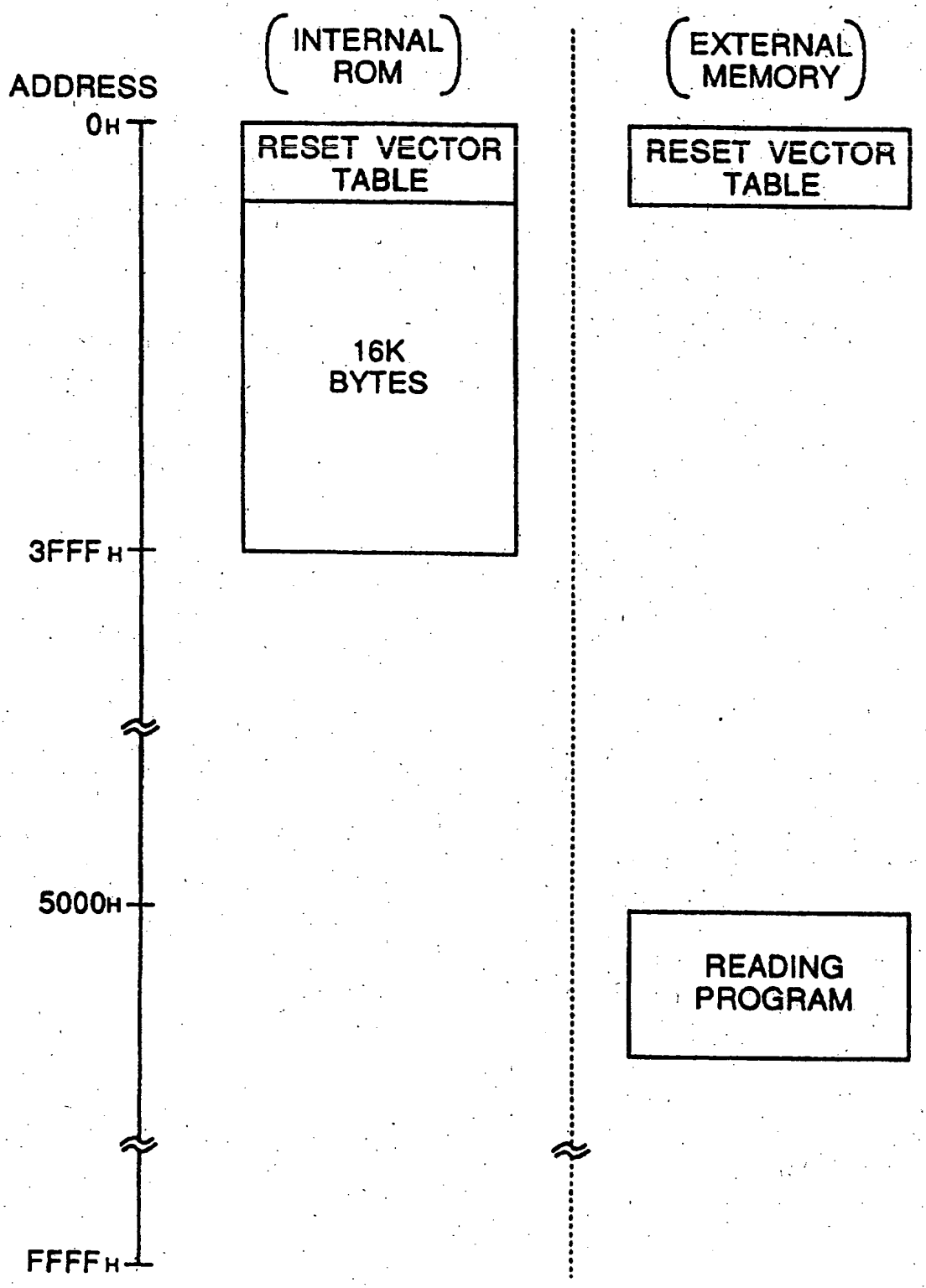

INTERNAL ROM
EXTERNAL MEMORY
ADDRESS
0H
RESET VECTOR TABLE
16K BYTES
RESET VECTOR TABLE
3FFFH
5000H
READING PROGRAM
FFFFH

FIGURE 3

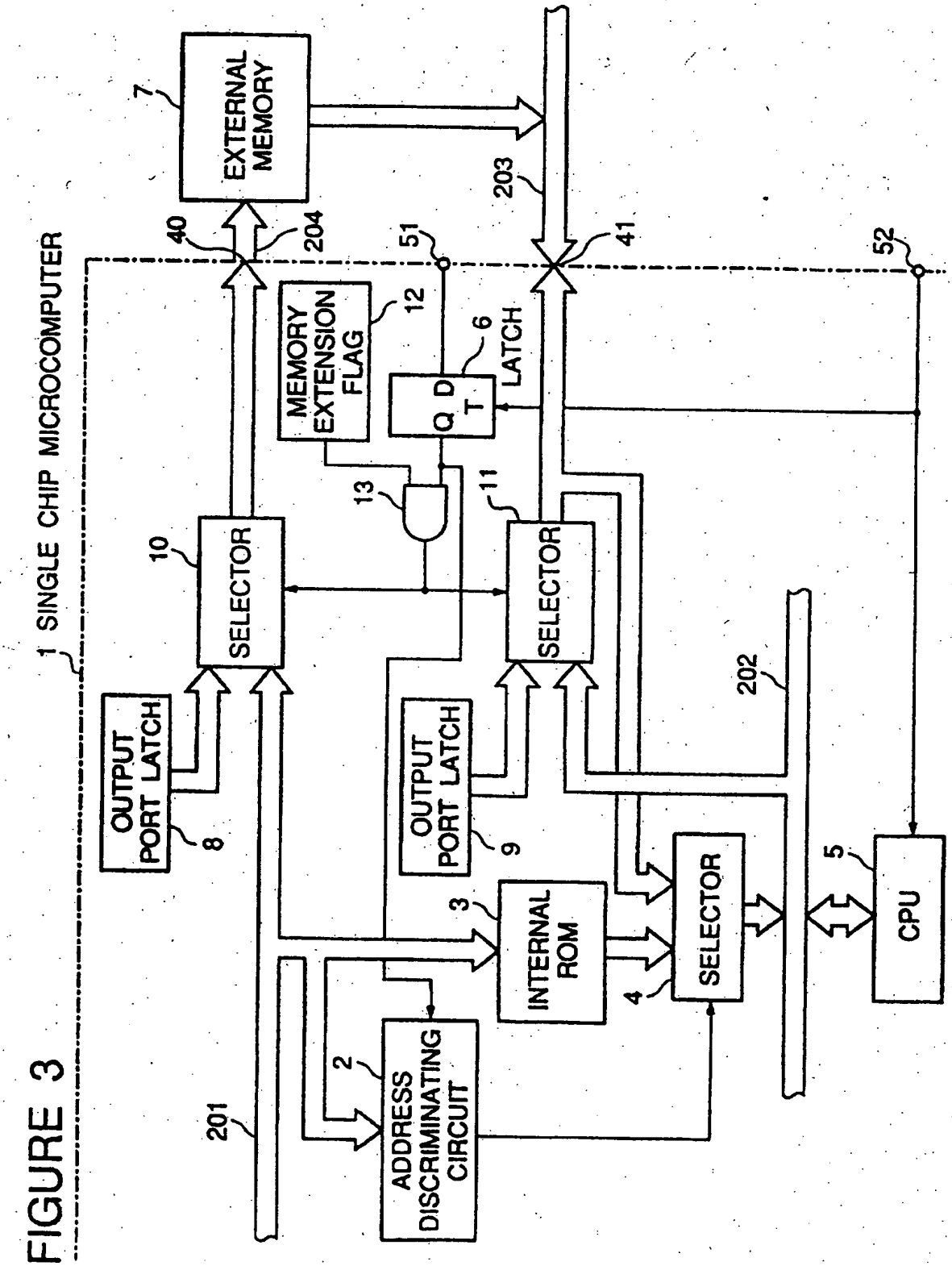
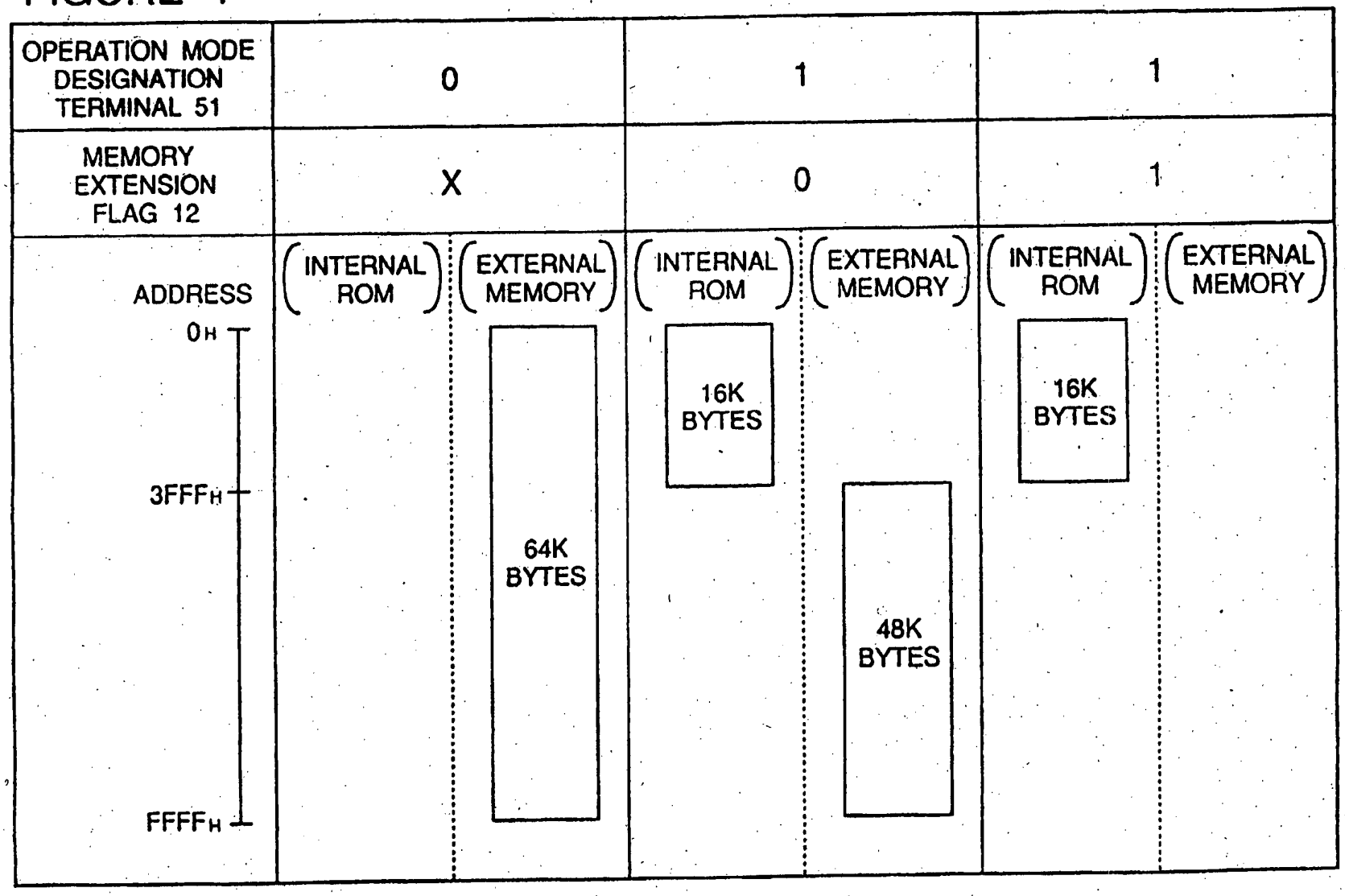

1 SINGLE CHIP MICROCOMPUTER
7
EXTERNAL MEMORY
203
40
204
51
41
52
MEMORY EXTENSION FLAG
12
6
LATCH
Q D
T
13
11
10
SELECTOR
SELECTOR
OUTPUT PORT LATCH
8
OUTPUT PORT LATCH
9
202
3
INTERNAL ROM
SELECTOR
5
CPU
4
2
ADDRESS DISCRIMINATING CIRCUIT
201

FIGURE 4


OPERATION MODE DESIGNATION TERMINAL 51
0
1
1
MEMORY EXTENSION FLAG 12
X
0
1
ADDRESS
0H
3FFFH
FFFFH
INTERNAL ROM
EXTERNAL MEMORY
64K BYTES
INTERNAL ROM
16K BYTES
EXTERNAL MEMORY
48K BYTES
INTERNAL ROM
16K BYTES
EXTERNAL MEMORY